UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/057,626	01/24/2002	Andrew Moroney	13453-002001	2191

42178 7590 03/03/2006

EMULEX DESIGN & MANUFACTURING CORPORATION
C/O MORRISON & FOERSTER LLP
555 WEST FIFTH STREET, SUITE 3500
LOS ANGELES, CA 90013

EXAMINER	
SERRAO, RANODHI N	

ART UNIT	PAPER NUMBER
2141	

DATE MAILED: 03/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/057,626	MORONEY ET AL.	
	Examiner	Art Unit	
	Ranodhi Serrao	2141	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 December 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2 and 4-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 4-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1, 2, and 4-16 have been considered but are moot in view of the new ground(s) of rejection.

2. The applicant argued in substance the amended claims 1, 5, 6, and 15. The new grounds teach these and the added features. See rejections below.

Claim Rejections - 35 USC § 103

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

4. Claims 1-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent to Radogna et al. (No. 5,991,299), U.S. Patent to Latif et al. (No. 6,400,730), and U.S. Patent to Satou et al. (5,717,946).

5. As per claim 1, Radogna et al. teaches a microsequencer system configured to translate said input data on the basis of said state information (see Radogna et al., col. 4, lines 25-50), the microsequencer system including at least one microsequencer (see Radog, col. 6, lines 19-36), said microsequencer system translating said input data into corresponding data expressed in said second network protocol (see Radogna et al., col. 8, lines 16-44). And Satou et al. teaches an instruction memory accessible to the at least one microsequencer of the microsequencer system, said instruction memory having a plurality of instruction words (see Satou et al., col. 57, lines 18-23), each of said instruction words forming a Very Long Instruction Word (VLIW) having a plurality of

instruction fields executable in parallel by different functional units of each at least one microsequencer (see Satou et al., col. 37, lines 29-44) to enable the at least one microsequencer to execute a plurality of instructions in a single instruction cycle (see Satou et al., col. 34, lines 20-28). But Radogna et al. and Satou et al. fail to teach a system for enabling communication between a first network having a first network protocol and a second network having a second network protocol, at least one of said first and second networks being a storage area network, said system comprising: a first data port for receiving input data from said first network said input data being expressed in said first network protocol; a second data port for receiving state information indicative of a state of a first storage area network selected from said first and second networks. However, Latif et al. teaches a system for enabling communication between a first network having a first network protocol and a second network having a second network protocol (see Latif et al., col. 2, lines 15-33), at least one of said first and second networks being a storage area network (see Latif et al., col. 3, line 47-col. 4, line 12), said system comprising: a first data port for receiving input data from said first network said input data being expressed in said first network protocol; a second data port for receiving state information indicative of a state of a first storage area network selected from said first and second networks (see Latif et al., col. 7, line 59-col. 8, line 9). It would have been obvious to one having ordinary skill in the art at the time of the invention to modify Radogna et al. and Satou et al. to a system for enabling communication between a first network having a first network protocol and a second network having a second network protocol, at least one of said first and second

networks being a storage area network, said system comprising: a first data port for receiving input data from said first network said input data being expressed in said first network protocol; a second data port for receiving state information indicative of a state of a first storage area network selected from said first and second networks in order to bring sophisticated SAN capabilities to existing enterprise computing configurations, without the installation of costly Fibre Channel switches and hubs, by providing the means for Internet Protocol (IP) devices to transparently communicate with SCSI and Fibre Channel devices over an IP network in an efficient manner (see Latif et al., col. 2, lines 15-33).

6. As per claim 2, Radogna et al., Latif et al., and Satou et al. teach a system, wherein said microsequencer system comprises at least one programmable microsequencer (see Radogna et al., col. 6, lines 19-36).

7. As per claim 4, Radogna et al., Latif et al., and Satou et al. teach a system, wherein said microsequencer system comprises a plurality of microsequencers configured to cooperate in translating said input data into corresponding data expressed in said second network protocol (see Radogna et al., col. 16, lines 36-54).

8. As per claim 5, Radogna et al., Latif et al., and Satou et al. teach an instruction-memory pointer for identifying a selected instruction word in said instruction memory (see Radogna et al., col. 6, lines 7-11).

9. As per claim 6, Radogna et al., Latif et al., and Satou et al. teach a system, further comprising a translation-memory accessible to the at least one microsequencer of said microsequencer system, said translation-memory having a translation-memory

address, and a translation-memory element corresponding to said translation-memory address, said translation-memory element including data for causing an instruction-memory pointer to jump to a selected instruction word (see Radogna et al., col. 9, lines 22-27).

10. As per claim 7, Radogna et al., Latif et al., and Satou et al. teach a system, wherein said translation-memory element is configured to include an absolute address of said selected instruction word (see Radogna et al., col. 9, line 29-col. 10, line 33).

11. As per claim 8, Radogna et al., Latif et al., and Satou et al. teach a system, wherein said translation-memory element is configured to include an offset from a current instruction word to said selected instruction word (see Radogna et al., col. 9, line 29-col. 10, line 33).

12. As per claim 9, Radogna et al., Latif et al., and Satou et al. teach a system, further comprising a translation-memory pointer for indirectly causing said instruction-memory pointer to jump to a selected instruction-memory address (see Radogna et al., col. 8, line 58-col. 9, line 5).

13. As per claim 10, Radogna et al., Latif et al., and Satou et al. teach a system, wherein said translation-memory pointer is configured to identify a selected translation-memory address corresponding to a translation-memory element that contains data indicative of said selected instruction-memory address (see Radogna et al., col. 8, line 58-col. 9, line 5).

14. As per claim 11, Radogna et al., Latif et al., and Satou et al. teach a system, further comprising a translation-memory having: a translation-memory address; a first

translation-memory element corresponding to said translation-memory address, said first translation-memory element including data for causing an instruction-memory pointer to jump to a first instruction word (see Radogna et al., col. 9, lines 22-27); a second translation-memory element corresponding to said translation-memory address, said second translation-memory element including data for causing said instruction-memory pointer to jump to a second instruction word (see Radogna et al., col. 15, line 65-col. 16, line 15); and a selector for selecting said first translation-memory element (see Radogna et al., col. 9, line 29-col. 10, line 33).

15. As per claim 12, Radogna et al., Latif et al., and Satou et al. teach a system, wherein said selector comprises a multiplexer having a first multiplexer input for receiving data indicative of content of said first translation-memory element; a second multiplexer input for receiving data indicative of content of said second translation-memory element (see Radogna et al., col. 5, lines 50-64); an output providing data selected from at least said first multiplexer input and said second multiplexer input; and a control input for controlling data provided at said output (see Radogna et al., col. 9, line 29-col. 10, line 33).

16. As per claim 13, Radogna et al., Latif et al., and Satou et al. teach a system, further comprising an output port in communication with said microsequencer system for providing said corresponding data to said second network (see Radogna et al., col. 12, lines 27-41).

17. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Radogna et al. and Satou et al.. Radogna et al. teaches a system for enabling

communication between a first network having a first network protocol and a second network having a second network protocol, said system comprising: a first input port for receiving input data from said first network; a second input port for receiving state information associated with said first network (see Radogna et al., col. 3, lines 1-22); a processing element in communication with said first and second input ports (see Radogna et al., col. 3, lines 23-33); an instruction memory accessible to said processing element, said instruction memory having a plurality of instruction words, (see Radogna et al., col. 6, lines 41-47), said plurality of instruction words being selected to translate input data from said first protocol to said second protocol (see Radogna et al., col. 11, line 51-col. 12, line 14); and an instruction-memory pointer for identifying a selected instruction word in said instruction memory (see Radogna et al., col. 6, lines 7-11). But fails to teach each of said instruction words forming a Very Long Instruction Word (VLIW) having a plurality of instruction fields executable in parallel by different functional units of the processing element to enable the processing element to execute a plurality of instructions in a single instruction cycle. However, Satou et al. teaches each of said instruction words forming a Very Long Instruction Word (VLIW) having a plurality of instruction fields executable in parallel by different functional units of the processing element (see Satou et al., col. 37, lines 29-44) to enable the processing element to execute a plurality of instructions in a single instruction cycle (see Satou et al., col. 34, lines 20-28). It would have been obvious to one having ordinary skill in the art at the time of the invention to modify Radogna et al. to each of said instruction words forming a Very Long Instruction Word (VLIW) having a plurality of instruction fields executable in

parallel by different functional units of the processing element to enable the processing element to execute a plurality of instructions in a single instruction cycle in order to efficiently execute instructions, therefore enabling the data string and bit map data to be executed quickly even when a low-cost slow memory system is connected thereto (see Satou et al., abstract).

18. Claims 14 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Radogna et al., Latif et al., and Satou et al. as applied to claims 1 and 15 above, and further in view of Muller et al. (6,453,360).

19. As per claim 14, Radogna et al., Latif et al., and Satou et al. teach the mentioned limitations of claim 1 above but fail to teach a system, wherein said first and second data ports and said microsequencer system are integrated into one integrated circuit. However, Muller et al. teaches a system, wherein said first and second data ports and said microsequencer system are integrated into one integrated circuit (see Muller et al., col. 8, lines 10-20). It would have been obvious to one having ordinary skill in the art at the time of the invention to modify Radogna et al., Latif et al., and Satou et al. to a system, wherein said first and second data ports and said microsequencer system are integrated into one integrated circuit in order to increase the efficiency of handling network traffic (see Muller et al., col. 4, lines 21-31).

20. As per claim 16, Radogna et al. and Satou et al. teach the mentioned limitations of claim 15 above but fail to teach a system wherein said processing element is selected from the group consisting of: a microsequencer system having at least one

microsequencer; a micro-processor; and an application-specific integrated circuit. However, Muller et al. teaches a system wherein said processing element is selected from the group consisting of: a microsequencer system having at least one microsequencer; a micro-processor; and an application-specific integrated circuit (see Muller et al., col. 8, lines 10-20 and col. 24, lines 12-25). It would have been obvious to one having ordinary skill in the art at the time of the invention to modify Radogna et al. and Satou et al. to a system wherein said processing element is selected from the group consisting of: a microsequencer system having at least one microsequencer; a micro-processor; and an application-specific integrated circuit in order to capitalize on the increased processor resources that are available in multi-processor computer systems (see Muller et al., col. 3, lines 29-42).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ranodhi Serrao whose telephone number is (571)272-7967. The examiner can normally be reached on 8:00-4:30pm, M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rupal Dharia can be reached on (571)272-3880. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SUPERVISORY PATENT EXAMINER